REMARKS

Claims 1-16, 34, 35, and 38-39 are all of the claims pending in the present Application. Claims 17-33 and 36-37 are canceled and claims 38-39 have been added. Claims Claim 9 is withdrawn from consideration until an allowable linking claim permits rejoinder.

It is noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

Claims 1-8, 10-16, and 34-37 stand rejected under 35 USC §112, first paragraph, as allegedly failing to comply with the written description requirement.

Claim 34 stands rejected under 35 USC §112, second paragraph, as allegedly being indefinite.

Claims 1-8, 10-16, and 34-37 stand rejected under the judicially-created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 2, and 4-17 in the parent Application 09/759,101, now U.S. Patent 6,653,240.

These rejections are respectfully traversed in view of the following discussion.

I. THE CLAIMED INVENTION

As described and claimed, for example, in claim 1, the present invention is directed to a method for circuit modification of a microelectronic chip comprising at least one conductor in an organic dielectric, in a manner so that a conductive residue from said ion-milling process does not contaminate said organic dielectric.

A protective inorganic surface layer is applied on the organic dielectric. A window is formed in the protective inorganic surface layer to selectively expose an underlying portion of the organic dielectric, the window being located over an area that covers a conductor to be modified by the ion-milling process. The organic dielectric is etched through the window to selectively remove a portion of the organic dielectric adjacent to the conductor.

The ion-milling process is performed on the conductor either to remove conductive material from the conductor to open up an existing routing in the circuit or to add conductive material to the conductor to form a new routing within the circuit.

As explained beginning at line 14 on page 1 of the specification, there is no conventional method that allows ion-milling to be used to modify circuits embedded in organic dielectric layer, since there is no known method that precludes the contamination of the organic dielectric layer during the ion-milling process. Without such method, as explained at lines 2-3 of page 2, ion-milling inherently utilizes charged ions that impregnate the organic dielectric to defeat electrical isolation.

In contrast, the present invention teaches that the organic dielectric layer be first selectively etched away from the conductor to be modified, so that the conductive residue from the ion-milling does not settle on the organic dielectric material adjacent to the operation. If necessary, the conductive residue from ion-milling process can specifically be also carried away by a passivation gas, such as xenon diflouride, introduced as part of the ion-milling procedure.

II. THE WRITTEN DESCRIPTION REJECTION

The Examiner rejects claims 1-8, 10-16, and 34-37 because the specification allegedly fails to describe that the conductive residue from the ion-milling does not contaminate the organic dielectric.

In response, Applicant respectfully directs the Examiner's attention to the following descriptions:

- line 20 of page 1 through line 3 of page 2: "*This conventional method of creating electrical disconnections is not applicable to organic dielectric/metallization schemes because no gas is commercially available that ensures the complete removal of residual metal, such as copper, in the milled area. More important, ion milling utilizes charged ions that impregnate the organic dielectric to defeat electrical isolation.*"

- lines 17-21 of page 3: "*With the invention, the problem in the prior art is overcome in which ion milling creates charged ions that impregnate the organic dielectric to defeat*

electrical isolation. The invention also overcomes the problem in the prior art of electrically conductive metal residue from ion milling being deposited on the sidewalls around the milled area, defeating electrical isolation."

- lines 9-15 of page 6: "*The wafer is then etched (S205) using a RIE process selective to the organic dielectric RIE gas mixtures for removing organic dielectrics contain varying amounts of oxygen. This etching is shown in Figure 1(b) as arrows 14, and the etching process results in a removal of the organic dielectric adjacent to targeted line 4, as shown by void area 16 and would typically remove the dielectric on each side of and partially below the targeted line to isolate the line from the surrounding dielectric.*"

Applicant believes that one having ordinary skill in the art would very clearly understand from the above-recited lines, particularly in combination with the void space indicated by the figures, that the selective removal of the organic dielectric adjacent to the portion of the conductor targetted to receive the ion milling processing solves the problem for ion milling of conductors embedded in organic dielectric layers. Clearly, because the void space has no organic dielectric, there are no charged ions impregnating any organic dielectric in this void space.

As explained at lines 5-6 of page 7, a gas assisted etch using xenon difluoride can be used for closely-spaced copper conductors, if needed, to assist to carry off the milled metal. As explained at lines 7-8 of page 7, an insulator such as SiO_2 is then deposited to fill the void space. Since the SiO_2 is applied after the milling process, it cleary does not have any ions impregnating it as resultant from the milling operation.

Therefore, Applicant believes that the specification very clearly describes that the step of etching out the void space around the conductor eliminates or at least reduces the problem in the art of residual metal and ion impregnation of the surrounding organic dielectric layers, and the Examiner is respectfully requested to reconsider and withdraw this rejection.

III. THE INDEFINITENESS REJECTION

The Examiner considers that the language of claim 34 is indefinite because it is unclear whether the ion milling is used to etch through the upper conductor.

In response, Applicant points out that the mechanism to cut through the upper conductor in order to expose the underlying lower conductor is not considered important, since any mechanism appropriate to the environment and composition of the upper conductor can be used.

Therefore, the Examiner is respectfully requested to reconsider and withdraw this rejection.

IV. THE REJECTION BASED ON DOUBLE PATENTING

Claims 1-8, 10-16, and 34-37 stand rejected under the judicially-created doctrine of obviousness-type double patenting over claims 1, 2, and 4-17 of the parent application, now US Patent 6, 653,240. Applicant again respectfully traverses this rejection.

That is, Applicant respectfully submits that the Examiner's current rejection has to be based only on the claim language of the claims of the parent application, further in view of the prosecution history. The Examiner clearly refused to allow claims of the parent application until Applicant incorporated into the independent claims the feature of exposing an underlying conductor. Therefore, the Examiner clearly considered the novelty of the claims of the parent application as necessitating this additional process of exposing the underlying conductor. The record is unclear how the Examiner's double-patenting rejection is based upon considering that a void is formed around the upper conductor in these independent claims of the parent.

In contrast to the claims of the parent application, the independent claims of the continuation application do not require that a second underlying conductor be exposed and, instead, defines that contamination of the organic dielectric is avoided by removing portion of the organic dielectric to form a void space adjacent to the conductor. Removing this organic dielectric material means that there is no organic dielectric material adjacent to the conductor that will be contaminated during the subsequent milling.

These independent claims are clearly entirely different from the feature of the independent claims of the parent, wherein the Examiner required for allowability that there is defined an additional step of exposing an underlying conductor. To establish an obviousness

rejection based on the claims of the parent application, the Examiner would have the initial burden of providing a reasonable prior art reference suggesting the void formed adjacent to the conductor, as described in the claims of the continuation that preclude contamination that would occur if this void were not present.

The Examiner fails to provide such prior art reference, let alone a reference to suggest recently-added dependent claim 35 and newly-added dependent claim 37.

Relative to the Examiner's position on the top of page 5 of the Office Action that at least one feature of the independent claims fails to have patentable weight because the Examiner is unable to find adequate coverage in the specification related to the prevention of contamination, Applicant has provided above the indications of locations in the specification of such coverage, thereby removing the basis for this position. It is noted that lack of written disclosure is not related to whether wording in a claim has patentable weight.

Relative to the Examiner's position in the first full paragraph on page 5 of the Office Action concerning the equivalence of the two conductors between recently-added dependent claim 34 and those of the independent claims of the parent, Applicant respectfully disagrees.

Taking independent claim 1 of the parent, US Patent 6,653,240, the upper conductor is clearly embedded in the organic dielectric, and the final claim limitation describes etching though an underlying layer to expose the lower conductor.

In contrast, dependent claim 34 of the continuation application clearly describes that the conductor of independent claim 1 is embedded in the organic dielectric and underlies an upper conductor. There is no suggestion in claim 34 that the upper conductor is similarly embedded in an organic dielectric layer. It may or may not be so embedded.

The case where the upper conductor is not embedded in an organic dielectric layer is clearly shown in Figure 3A, as described in lines 12-18 on page 7, wherein surface conductor 32 is clearly described as an Mx copper wide line, and there would be no need to etch out a void around this surface conductor 32 prior to cutting a working hole through the surface conductor 32 enroute to reaching an underlying conductor that is embedded in an organic dielectric layer.

Thus, recently-added dependent claim is indeed different from the two-conductor scenario of the independent claims of the parent and is clearly not obvious from the claims of the parent without extensive rationale not currently of record.

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this double patenting rejection, particularly in view of the undue delay of the USPTO in taking up prosecution of the continuation application. Applicant respectfully submits that such undue delay warrants the effect of a term adjustment, particularly in view that the prior art rejection relied upon for the parent rejection was never fully justified on the record.

V. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-16, 34, 35, and 38-39, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance, since withdrawn claim 9 would be subject to rejoinder. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 09-0458.

Respectfully Submitted,

Date: February 19, 2008

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